In the Claims

The following listing of claims replaces all prior listings and versions of claims in this application.

1-32. (Canceled)

33. (New) A processor comprising:

a subcircuitry configured to perform a sign extension associated with a sign extension field value of a multi-byte non-branch instruction, wherein said subcircuitry is further configured to perform a sign extension associated with a sign extension field value of a multi-byte branch instruction, wherein said subcircuitry is operable to use the multi-byte branch instruction to bypass access to a first byte of a multi-byte target instruction to access another byte of the multi-byte target instruction.

34. (New) The processor of claim 33, wherein the multi-byte branch instruction is one word in length, and wherein the multi-byte non-branch instruction is one word in length.

35. (New) The processor of claim 33, wherein the target instruction is one word long.

36. (New) The processor of claim 33, wherein the multi-byte branch instruction comprises a conditional branch instruction.

37. (New) The processor of claim 33, wherein the multi-byte branch instruction comprises a branch offset and a program counter value.

38. (New) The processor of claim 37, wherein each of the branch offset and the program counter value have a unit of a byte.

39. (New) The processor of claim 33, wherein said subcircuitry is operable to access the multi-byte target instruction at a byte from an address of the multi-byte target instruction.

40. (New) The processor of claim 33, wherein the processor includes a field programmable gate array.

41. (New) The processor of claim 33, wherein the sign extension field value of the multi-byte branch instruction is one or more bytes.

42. (New) The processor of claim 33, further comprising a receiving component configured to receive the multi-byte branch instruction and the multi-byte non-branch instruction.

43. (New) A method comprising:

performing a sign extension associated with a sign extension field value of a multi-byte non-branch instruction;

performing a sign extension associated with a sign extension field value of a multi-byte branch instruction, wherein the sign extensions associated with the multi-byte non-branch and branch instructions are performed by a component; and

accessing a byte of a multi-byte target instruction by bypassing a first byte of the multi-byte target instruction and by using the multi-byte branch instruction.

44. (New) The method of claim 43, further comprising:

accessing the multi-byte branch instruction that is one word in length; and

accessing the multi-byte non-branch instruction that is one word in length.

45. (New) The method of claim 43, wherein said accessing the byte of the multi-byte target instruction comprises reading the byte.

46. (New) The method of claim 43, wherein said performing the sign extension associated with the sign extension field value of the multi-byte branch instruction comprises performing the sign extension associated with the sign extension field value of a multi-byte conditional branch instruction.

47. (New) The method of claim 43, further comprising:

accessing a branch offset having a unit of a byte in the multi-byte branch instruction; and

accessing a program counter value having a unit of a byte in the multi-byte branch instruction.

48. (New) The method of claim 43, wherein said accessing the byte of the multi-byte target instruction comprises accessing the byte of a word long target instruction.

49. (New) The method of claim 43 wherein said accessing the byte of the multi-byte target instruction comprises accessing the byte at a byte from an address of the multi-byte target instruction.

50. (New) The method of claim 43, wherein said performing the sign extension associated with the sign extension field value of the multi-byte branch instruction comprises performing the sign extension of the sign extension field value having one or more bytes.

51. (New) The method of claim 43, further comprising receiving the multi-byte branch instruction and the multi-byte non-branch instruction.

52. (New) A computer readable medium having instructions stored thereon that, if executed by a computing device, cause the computing device to perform a method comprising:

performing a sign extension associated with a sign extension field value of a multi-byte non-branch instruction;

performing a sign extension associated with a sign extension field value of a multi-byte branch instruction, wherein the sign extensions associated with the multi-byte non-branch and branch instructions are performed by a component; and

accessing a byte of a multi-byte target instruction by bypassing a first byte of the multi-byte target instruction and by using the multi-byte branch instruction.

53. (New) The computer readable medium of claim 52, wherein said method further comprises:

accessing the multi-byte branch instruction that is one word in length; and

accessing the multi-byte non-branch instruction that is one word in length.

54. (New) The computer readable medium of claim 52, wherein said accessing the byte of the multi-byte target instruction comprises reading the byte.

55. (New) The computer readable medium of claim 52, wherein said performing the sign extension associated with the sign extension field value of the multi-byte branch instruction

comprises performing the sign extension associated with the sign extension field value of a multi-byte conditional branch instruction.

56. (New) The computer readable medium of claim 52, wherein said method further comprises:

accessing a branch offset having a unit of a byte in the multi-byte branch instruction; and

accessing a program counter value having a unit of a byte in the multi-byte branch instruction.

57. (New) The computer readable medium of claim 52, said accessing the byte of the multi-byte target instruction comprises accessing the byte of a word long target instruction.

58. (New) The computer readable medium of claim 52, wherein said accessing the byte of the multi-byte target instruction comprises accessing the byte at a byte from an address of the multi-byte target instruction.

59. (New) The computer readable medium of claim 52, wherein said performing the sign extension associated with the sign extension field value of the multi-byte branch instruction comprises performing the sign extension of the sign extension field value having one or more bytes.

60. (New) The computer readable medium of claim 52, wherein said method further comprises receiving the multi-byte branch instruction and the multi-byte non-branch instruction.